Pattern matching is a crucial task in several critical network services such as intrusion detection and matching of the IP address during packet forwarding by the router. In this paper we present an speed vs area tradeoff of the the original DFA and the DFA called delayed input DFA (D2FA) with optimized area by eliminating the redundant transition edges. In delayed input DFA the area required to store transition table reduces to 60% of the original DFA but the clock pulse required to execute the process increases almost 40% of the original DFA. The comparison of area and speed is presented. This area optimized architecture of DFA is simulated and synthesized using VHDL on the Xilinx ISE 12.4.

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Efficient String Matching Using Deterministic Finite Automation Hardware: Speed vs Area Tradeoff

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Index Terms

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Keywords

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