Abstract

Pattern matching is a crucial task in several critical network services such as intrusion detection and matching of the IP address during packet forwarding by the router. In this paper we present an speed vs area tradeoff of the the original DFA and the DFA called delayed input DFA (D2FA) with optimized area by eliminating the redundant transition edges. In delayed input DFA the area required to store transition table reduces to 60% of the original DFA but the clock pulse required to execute the process increases almost 40% of the original DFA. The comparison of area and speed is presented. This area optimized architecture of DFA is simulated and synthesized using VHDL on the Xilinx ISE 12.4.

References

- A. BabuKaruppiah, Dr. S Rajaram "Deterministic Finite Automata for Pattern Matching in FPGA for intrusion Detection" in International Conference on Computer and Electrical Technoogy-ICCCET 2011, 18th & 19th March, 2011. 
- Jan Kastil, Jan Korenek Hardware Accelerated Pattern Matching Based on Deterministic Finite Automata with Perfect Hashing IEEE 2010, p-149-152.
- Kai Wang, Yaxuan Q, Yibo Xue, Jun LRorganized and Compact DFA for Efficient Regular Expression Matching, IEEE communication society
Efficient String Matching Using Deterministic Finite Automation Hardware: Speed vs Area Tradeoff

- Hoang Le and Viktor K. Prasanna Ming Hsieh Department of Electrical Engineering University of Southern California Los Angeles, CA 90089, USA A Memory-Efficient and Modular Approach for String Matching on FPGAs, 2010.
- B. L. Hutchings and R. Franklin and D. Carver "Scalable hardware implementation usonf Finite Automata" Department of Electrical and Computer Engineering.

Index Terms

Computer Science

Keywords

String Matching dfa Vhdl