Abstract

An 8-bit programmable square finder cum frequency divider architecture is presented. This special architecture includes a high speed parallel counter, clock trigger circuit, eight bit multiplier logic, sequence termination logic and sequence restarter logic. The entire architecture is divided into two parts: The frequency divider section and the square finder section. The frequency divider circuit outputs a sequence of states and the modulus is determined by the external frequency select input. The Square finder circuit finds the square of the given number by repetitively adding the number that much times. The counter consists of two main sections- the counting section and the state Anticipation Module. The 8-bit square finder cum frequency divider employing existing counter architecture [5] consumes a total transistor count of 1206 whereas the same using proposed counter architecture consumes only 1038. The worst case delay of the proposed programmable square finder cum frequency divider architecture employing the existing and proposed counter architecture was found to be 21.829ns and 20.686 respectively and the Power dissipation at 250 MHz was found to be 6.35 mW and 5.77mW respectively.

References

- Yuan, J. R. "Efficient CMOS Counter Circuits," Electronics Letters, vol. 24,
A High Speed Parallel Counter Architecture and its Implementation in Programmable Squar...
High Speed Parallel Counter Architecture

Counter  Square  Frequency Divider  High Speed  State Anticipation Module  Sequence  Modulus