Abstract

Reversible logic is an emerging research area. Interest in this field is motivated by its applications in several technologies involving low voltages and low power. Binary reversible circuits have been studied for their potential application in low-power CMOS design, quantum computation, nanotechnology, optical computation, etc. In this paper, a Reversible low power Decoder is proposed, newly proposed decoder compared with already proposed reversible decoder and the Conventional decoder. Circuits have been designed and synthesized using Rev Kit. The circuits are simulated in cadence too and Power consumption is calculated using cadence for all three designs. The performance analysis is verified using number of reversible gates, Garbage outputs, Transistor cost, Line cost power consumed and Quantum Cost. Improvement in the area of the proposed decoder as compared to the conventional one can be shown to be 33.33% and total power of 9.44%. Also an algorithm for NX2N decoder is given.
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**Index Terms**

Computer Science
Integrated Circuits

**Keywords**
Feynman Gate  Fredkin Gate  Garbage Output  Line Cost  Quantum Cost  Reversible Logic.