Abstract

Multirate DSP systems in which different parts at different sampling rates. The increase in the sampling interval results in more time available for processing. Decimation generally includes first low-pass filtering the signal and then discarding some of the samples. Zero stuffing is performed in the process of interpolating a discrete-time signal, and then low-pass filtering the resulting signal. The proposed decimator is implemented using MATLAB as standard FIR, Half Band FIR and Nyquist FIR by using the multistage design techniques. The performance of different decimator designs is compared in terms of error and hardware requirements. The results show that the performance of all designs is almost identical but their implementation cost varies greatly in terms of hardware requirements. The hardware saving of 49% to 84% can be achieved by using multistage Nyquist decimator design. Reduced computational work load, lower filter order, lower coefficient sensitivity and noise and less stringent memory requirements.

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Index Terms

Computer Science  
Signal Processing

Keywords
Zero-stuffing  Decimation  Music aliasing