Abstract

Recent advancement in the semiconductor technology allow the hardware engineers to integrate complex modules like processors, peripheral devices, and memory in a single System-on-a-Chip (SoC); where testability, power minimization and management, area minimization are the important system level considerations. Performances both in terms of processing speed and power consumption are becoming more and more challenging in SOC designing. Novel system on chip architectures should be able to execute multiple performances demanding applications while maintaining low power consumption, small area, non-recurring engineering costs and short time to-market. Hence a lot of research is going on to implement CGRA in SOC because Coarse-grained reconfigurable architecture can provide both performance and flexibility. This paper gives a guided tour over a decade of development in CGRA and their significance in SOC design

References

- A dynamically reconfigurable system-on-a-chip architecture for future mobile digital signal processing (1999) by Ahmad Alsolaim, Jürgen Becker European signal processing conference
Survey on Coarse Grained Reconfigurable Architectures


Index Terms

Computer Science

Architecture
Keywords

Chess Architecture  Reconfigurable Pipelined Datapath (rapid)  Dynamically Reconfigurable Architecture For Mobile Systems (dream)

Adres (architecture For Dynamically Reconfigurable Embedded System)

Mora (multimedia Oriented Reconfigurable Array)

Dynamically Reconfigurable Mac Processor (drmp)