Abstract

The need of high speed multiplier is increasing as the need of high speed processors are increasing. A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction. This paper presents a high speed 4x4 bit Vedic Multiplier (VM) based on Vertically & Crosswise method of Vedic mathematics, a general multiplication formulae equally applicable to all cases of multiplication. It is based on generating all partial products and their sum in one step. The coding is done in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) while the synthesis and simulation is done using EDA (Electronic Design Automation) tool - XilinxISE12.1i. The combinational path delay of 4x4 bit Vedic multiplier obtained after synthesis is compared with normal multipliers and found that the proposed Vedic multiplier circuit seems to have better performance in terms of speed.

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Design of 4x4 bit Vedic Multiplier using EDA Tool

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