Abstract

A Priority Interrupt Controller is a hardware designed chip which acts as an overall system manager to efficiently handle the multiple interrupts that tend to occur from the varied number of peripheral devices. Hence, it relieves the system's CPU from the task of polling in a multilevel priority system. This paper deals with implementation of a Priority Interrupt Controller using Verilog language. During the implementation, the Verilog code has been written for all the internal registers of the Priority Interrupt Controller so that it can accomplish its task of prioritizing the various interrupts and thereby increasing the efficiency of the processor. In this paper the entire functional block was sub divided into various modules like vector address module, command register module, mask register module and finally it was integrated into a single unit to accomplish specified tasks. In the present work the Priority Interrupt Controller was made to operate in three different modes-Fully Nested Mode, Rotating Priority Mode, and Special Mask Mode.

References

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**Index Terms**

Computer Science  
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**Keywords**

Fpga  Fully Nested Mode  Interrupt Controller  Rotating Priority Mode  Special Mask Mode