Abstract

Transferring data between two points is very essential, also the accuracy of the transferred data is vital for some critical applications, but an error during the transmission of data is very common. The Cyclic Redundancy Check (CRC) method is generally used for error detection and correction. In this paper, we have proposed a new technique for error detection and correction in case of CRC-16, which is hardware optimized and works at relatively higher frequency and speed. In the proposed method, it is possible to detect the exact place of single bit error and correct them using minimum hardware. This method involves no look tables and hence is memory efficient. This paper focuses on effective implementation of this method on FPGA.

References

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**Index Terms**

Computer Science
Communications

**Keywords**

CRC  Field Programmable Gate Array  Single bit error correction  Parallelism  non-lookup technique