Abstract

VLSI Design looking towards to solve design constructions that arises when using clock pulses. The majority of the constrains can be overcome by using asynchronous logic, additionally synchronous circuits has some inherent advantages over synchronous counterparts. This paper demonstrates the design of efficient asynchronous pipelines for some standard logic circuits and medium scale integration (MSI) circuits. The performance analysis of various templates is designed for different standard logics and MSI circuits. The QDI templates are highly tolerant of process variations due to the up and down transitions are sensed. QDI circuits are quite robust in terms of process variations and design tolerances. In this work, expose a timing assumption used in staticizers for QDI logic and apply it to other parts of circuits. Goal of this work is to optimize circuits with respect to area and power while maintaining the robustness.

References

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Index Terms

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