Abstract

In this paper a hybrid approach is presented to design and implement a GSM digital down converter for enhanced resource utilization. The proposed DDC has been implemented by hybridizing the multiplier less and multiplier based decimators. A multiplier less CIC decimator has been used to reduce the cost by reducing the multiplier requirement. Two computationally efficient equiripple polyphase decomposition structure based decimators have been to reduce the filter order and hardware complexity. The embedded multipliers, LUTs and BRAMs have been efficiently utilized to enhance the system performance and resource utilization. The proposed GSM DDC has been designed and simulated Matlab and Simulink, synthesized with Xilinx Synthesis Tool and implemented on Virtex-II Pro based xc2vp20 FPGA device. The proposed design has shown a minimum period of 159.96 MHz with enhance resource utilization ranging from 4-12 % in terms slices, flip flops LUTs, BRAMs and multipliers.

References

**Index Terms**
- Computer Science
- Signal Processing

**Keywords**
- BRAM
- DDC
- FPGA
- LUT
- GSM