Abstract

In this work, a 4-bit pipelined ADC that provides the high speed conversion needed in UWB applications with sampling frequency of the order 50 Gbps is proposed. The pipelined ADC designed uses a high speed 1-bit comparator, wide band amplifier, sampling circuit and a high speed buffer. The individual blocks are designed using 130nm CMOS low power library cells. The individual blocks are designed to operate at a frequency greater than 50 Gbps sampling rate. In order to operate increase the operating frequency of the pipelined ADC, Specific new design techniques/algorithms such as power-efficient, capacitor ratio-independent conversion scheme, a pipeline stage-scaling algorithm, a nested CMOS gain-boosting technique, an amplifier and comparator sharing technique, and the use of minimum channel-length, thin oxide transistors with clock bootstrapping and in-line switch techniques are adopted.

References

- J. H. Reed (Editor), "An introduction to ultra wideband communication systems," Prentice Hall, 2005
VLSI Implementation of 4-bit 50Gbps High Speed Pipelined ADC Architecture for I-UWB Receiver


Index Terms

Computer Science Integrated Circuits

Keywords
I-UWB receiver  pipelined ADC  high speed  CMOS gain boosting  clock boot strapping