Abstract

Parallel prefix adder is the most flexible and widely used for binary addition. Parallel Prefix adders are best suited for VLSI implementation. A number of parallel prefix adder structures have been proposed over the past years intended to optimize area, fan-out, logic depth and inter connect count. This paper presents a hybrid high speed and area efficient adder architecture, based on parallel prefix computation by using four operators namely black, gray, O3-black and O3-gray operators. These operators are designed using multiplexers. The proposed hybrid architecture is implemented with 16-bit width operands on Xilinx Spartan 3E FPGA. The experimental results indicate that the proposed architecture is much faster and area efficient.

References

Design and implementation of a Hybrid High Speed Area Efficient Parallel Prefix Adder in an FPGA


**Index Terms**

Computer Science

Integrated Circuits
Keywords