Abstract

Scaling of transistor features sizes has improves performance, increase transistor density and reduces the power consumption. A chip’s maximum power consumption depends on its technology as well as its implementation. As technology scales down and CMOS circuits are powered by lower supply voltages, leakage current becomes significant. Static power is becoming the predominant source of energy waste. To create methodologies that support efficient designs, good performance, lower costs in the era of low power, is up to the design, EDA community. As the threshold voltage is reduced due to scaling, it leads to increase in sub threshold leakage current and hence increase in static power dissipation. This paper presents performance analysis of inverter using conventional CMOS, stack and dual threshold transistor stacking techniques. The performance analysis of inverter were analyzed in 90nm technology using Cadence virtuoso environment. The use of dual threshold voltages can significantly reduce static power dissipated in CMOS VLSI circuits.

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**Index Terms**

Computer Science Integrated Circuits

**Keywords**

CMOS inverter static power threshold voltage transistor stacking ULSI ifx