Abstract

This paper discusses combined software and hardware architecture of a H. 264/AVC video compression decoder. The software version of the decoder was implemented using NIOS II processor on a FPGA board (Stratix III of Altera). The mixed, software and hardware, architecture was proposed to ameliorate the decoder speed throughputs. According to the time execution profiling and data dependencies, the decoder partitioning was applied. Thus, the inverse 4x4 Intra process is replaced by a hardware accelerator. It includes inverse 4x4 Intra prediction, inverse transform and inverse quantization. The experimental results at 317 MHz show improvement on the decoding throughput by 20% between software solution and mixed one.
References

- Damak T., Werda I., Samet A., Masmoudi N., &quot;DSP CAVLC implementation and Optimization for H. 264/AVC baseline encoder&quot;, IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2008, MALTA.


- Stratix III device, http://www.altera.com/


**Index Terms**

Computer Science  Multimedia

**Keywords**

H. 264 /AVC decoder  software and hardware implementation  inverse 4x4 intra prediction  inverse transform

inverse quantization