Abstract

This paper discusses combined software and hardware architecture of a H. 264/AVC video compression decoder. The software version of the decoder was implemented using NIOS II processor on a FPGA board (Stratix III of Altera). The mixed, software and hardware, architecture was proposed to ameliorate the decoder speed throughputs. According to the time execution profiling and data dependencies, the decoder partitioning was applied. Thus, the inverse 4x4 Intra process is replaced by a hardware accelerator. It includes inverse 4x4 Intra prediction, inverse transform and inverse quantization. The experimental results at 317 MHz show improvement on the decoding throughput by 20% between software solution and mixed one.
References

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