Abstract

This paper introduces a new technique for reducing glitches in logic circuits implemented on Field Programmable Gate Arrays (FPGAs). The technique is based on the principles of path balancing. The main objective was to achieve glitch minimization which, in turn, would reduce dynamic power during routing on FPGAs. The glitch aware routing was adopted for simulations tests. The input paths to look-up table (LUT) are balanced by aligning signals so that all input signals arrive simultaneously at LUT. To perform simulation tests and validation of new design, two different benchmark logic circuits of adder and multiplier were considered for implementation on FPGAs. Simulated results; analyses of selected benchmark circuits showed that there was a reduction in dynamic power consumption by FPGAs by about 11.5% and 7.5% for LUT input size of 16 bits, for adder and multiplier circuits respectively. The improvements in power consumptions are based on the computations for glitch aware router with path balancing compared to that of glitch unaware routers.

References

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Index Terms

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