Abstract

The increasing complexity of algorithms and embedded systems constraints has lead to advanced design methodologies. Hardware/Software co-design methodology has made it possible to find an optimal architecture for a given application by exploring the design space before building a real hardware prototype. The Design Space Exploration is basically exploring the various processor architectures in order to search for a processor architecture that satisfies different conflicting criteria such as chip area, speed, power consumption or on-chip memory requirements. The output is a set of different architectures representing the different tradeoffs. Retargetable compiler is an important tool in design space exploration (DSE). Retargetable compiler is capable of generating code for different target processors, by reusing most of the code. The objective of this research is to develop a retargetable compiler that can generate efficient code in terms of code size, cycle count and retargetability efforts for a VLIW processor.

Index Terms
Computer Science Embedded Systems

Keywords
Retargetable Compilers VLIW ILP