Abstract

An 8-bit 10 MS/s SAR A/D converter is presented. In the circuit design, a capacitor switched D/A Converter architecture, Dynamic latched comparator architecture and low power SAR logic are utilized. Design challenges and considerations are also discussed. This proposed converter is implemented based on 0.29um CMOS logic process. With a 3.3 V analog supply and a 5 V digital supply, the differential and integral nonlinearity are measured to be less than 0.36 LSB and 0.69 LSB respectively. With an input frequency of 625 KHz at 10 MS/s sampling rate and the power dissipation is measured to be 6.62 mW.

References

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Index Terms

Computer Science

Circuits And Systems

Keywords

Analog to Digital Converters (ADC)  Digital to Analog Converter (DAC)  Successive Approximation Registers (SAR)

Comparator

Latch