Abstract

An 8-bit 10 MS/s SAR A/D converter is presented. In the circuit design, a capacitor switched
D/A Converter architecture, Dynamic latched comparator architecture and low power SAR logic
are utilized. Design challenges and considerations are also discussed. This proposed
converter is implemented based on 0.29um CMOS logic process. With a 3.3 V analog supply
and a 5 V digital supply, the differential and integral nonlinearity are measured to be less than 0.
36 LSB and 0.69 LSB respectively. With an input frequency of 625 KHz at 10 MS/s sampling
rate and the power dissipation is measured to be 6.62 mW.
- B. Razavi and B. A. Wooley, "A 12-b 5-MSample/s Two-Step CMOS A/D
- F. Maloberti, Design of analog-digital VLSI circuits for telecommunications and signal
  processing, Layout of Analog and Mixed Analog-digital Circuits, Prentice Hall, second edition,
- M. J. M. Pelgrom, A. C. J. Duenmaijer and A. P. G. Welbers, "Matching
  1989.
- P. M. Figueiredo and J. C. Vital, "Kickback Noise Reduction Techniques for
- M. D. Scott, B. E. Boser and K. S. J. Pister, "An Ultralow-Energy ADC for

Index Terms

Computer Science

Circuits And Systems

Keywords

Analog to Digital Converters (ADC)  Digital to Analog Converter (DAC)  Successive
Approximation Registers (SAR)

Comparator

Latch