Abstract

CMOS refers to both a particular style of digital circuit design and the family of processes used to implement that circuitry on an integrated circuit (chips). Due to the low power dissipation by the MOS devices, the use of them is quite prominent in the VLSI. Semiconductor technology based Dual Modulus Prescaler is to be fabricated in 90 nm technology. It basically comprises of 2 blocks for controlling the pulses generated at the output i.e. 256 or 257. The synchronous divide-by-4/5 divider uses symmetric fashion D flip-flops to achieve more than 10 GHz maximum operating frequency. Also the technology that has been used for construction of the D flip flop is of most basic components i.e. the nMOS gates and the inverters. Here, the inverters are constructed by using the NAND gates. This has simply done by shorting the two terminals of the NAND gate and making it as an inverter. The same can be done by using nor or any other gate too. The use of this design will make the consumption of the power in microwatt as the source couple logic used in the previous design concepts has power consumption in mW [1]. This modules output is to be carried out by using the Micro wind software 3.1. The prescaler will require upto 1.2-V supply. The prescaler's estimated operating frequency is upto 17 GHz.
A Survey Paper on Semiconductor Technology based Dual Modulus Prescaler

References


Index Terms

Computer Science
Integrated Circuits

Keywords

Dual modulus prescaler  CMOS  low power