Abstract

Network on Chips (NoCs) replace traditional busses in highly integrated Multiprocessor System on Chips (MPSoCs). As SoCs, communication issues take much important in NoCs but they need to give contention free architecture with low latency. To meet the above need several methods like handshaking mechanism and arbiter designs developed and implemented. This paper presents various scheduler designs using iSLIP scheduling algorithms and its comparative analysis with various arbiters. All the arbiters described using Verilog HDL and synthesized using Xilinx. For performance analysis, Cadence RTL compiler with UMC 0.13µm technology used to compute power and area of all the algorithms for arbiter.

References


Index Terms

Computer Science  Information Systems

Keywords

SoCs  MPSocs  Communication latency  scheduling algorithms  arbiter