Abstract

In this paper, we propose a low-cost sequential architecture for the implementation of CORDIC algorithm in two computation modes. It suited for serial operation that performs conversion between polar and rectangular coordinate systems, essentially sin/cos, sinh/cosh and arctan computation. The design targets real time application of fingerprint recognition. We present a VHDL description of CORDIC algorithm. To reduce iteration delay, we used some combinatorial blocks. Fixed point arithmetic was considered. To validate our conception and its CORDIC accuracy, we present relative error calculated in convergence range for some trigonometric and hyperbolic functions. All measurements show an enhancement compared with our previous work. The architecture was implemented and tested. The contribution of the paper includes the CORDIC design flow.
FPGA Implementation of the CORDIC Algorithm for Fingerprints Recognition Systems

References


Index Terms

Computer Science
Pattern Recognition

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Keywords
CORDIC algorithm  fingerprint  VHDL  hardware  FPGA