Abstract

In this paper a method to build a faster array multiplier based on Radix 4 Modified Booth Encoder - which is broadly used for the signed multiplication applications- with less area and power is presented. This is achieved by optimizing the overall interconnection delay in the partial product array and by scheming the most efficient Full Adder and Booth Encoder in Complementary Pass Transistor Logic approach. The proposed array multiplier’s performance in terms of delay, power and area is compared with conventional as well as Baugh-Wooley Multiplier. In order to optimize the power and area of the multiplier, a CPL Based MBE with standard partial product array is proposed and designed in full custom style. The use of efficient 10 Transistor based Full adders based on CPL logic ensures that the entire design is in CPL logic, which provides a regular outline with less interconnection intricacy.

References

- A. D. Booth, "A signed binary multiplication technique," Quarterly Journal of...

**Index Terms**

- Computer Science
- Integrated Circuits
**Keywords**

Modified Booth Encoder  Array Multiplier  Radix-4 Multiplier  Low Power multiplier

Fast Multiplication