Abstract

In the modern technology of communication architecture, network on chip is widely used as communication architecture. Network on chip topologies are becoming a backbone of communication architectures. Network on chip provides a good integration of huge amount of storage on chip blocks as well as computational also. Network on chip handled the unfavorable conditions and it provides the scalability to the architecture. Mesh and folded torus architectures are most commonly used architecture for network on chip communication. Here, we compare the performance of Mesh and Folded torus network architecture on chip, on the basis of different parameters under broadcasting with the help of distance vector routing algorithm. To evaluate the performance of Mesh and folded torus network on chip in the simulation environment, we use the network simulator (NS-2) in the Linux platform.

References

- L. Benini and G. De Micheli, "Networks on chip: a new paradigm for systems on
Performance Comparison of Mesh and Folded Torus Network under Broadcasting, using Distance Vector Routing Algorithm

- Sameer Bataineh, Ajmad Odet-Allah, Raed Al-Omari, "Reliability of mesh and torus..."
- Yi-Ran Sun, Shashi Kumar, Axel Jantsch, “Simulation and Evaluation for a Network on Chip Architecture Using NS-2”; the Department of Microelectronics & Information Technology (IMIT).

Index Terms

Computer Science | Data Communication

Keywords
<table>
<thead>
<tr>
<th>Network on chip</th>
<th>Performance</th>
<th>Mesh</th>
<th>Folded Torus</th>
<th>Latency</th>
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