Modified Optimal Performance Mapping on Reconfigurable Architecture for Multimedia Applications

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Abstract

In this paper, Coarse-grained reconfigurable architectures (CGRAs) are capable of achieving both goals of high performance and flexibility. CGRAs not only improve performance by exploiting the features of repetitive computations, but also can adapt to diverse computations by dynamically changing configurations of an array of its internal processing elements (PEs) and their interconnections. This paper introduces approaches to mapping applications onto CGRAs supporting both integer and floating point arithmetic. After presenting an optimal formulation using integer linear programming, we present a fast heuristic mapping algorithm. Our experiments on randomly generated examples generate optimal mapping results using our heuristic algorithm for 97% throughput. We observe similar results for practical examples from multimedia and 3-D graphics benchmarks. The applications mapped on a CGRA show up to 120 times performance improvement compared to software implementations, demonstrating the potential for application acceleration on CGRAs supporting floating-point operations. ISE Xilinx 9.1 version, Altra ModelSim SE 5.7. was used to simulate and verify the results.

References


Index Terms

Computer Science Multimedia

Keywords

Design automation, high-level synthesis, parallelizing compiler, reconfigurable architecture. CGRAs