Abstract

This paper represents 2048 point Fast Fourier Transform and its inverse (FFT/IFFT) for Mobile Wi-MAX. Modified architecture also provides concept of local ROM module and variable length support from 128–2048 point for FFT/IFFT. UMC 0.18µm is used to design the same. FFT/IFFT chip consumes 266.81mW at 40MHz, 130.74mW at 20MHz and 65mW at 10 MHz for length of 2048 point. Its core size is 2.6mm x 2.6mm. Its latency is 2050 clock cycle with maximum clock frequency 40MHz. Start up time for the chip is N/2 clock cycle where N is the length of FFT/IFFT. 16 bit word length with fixed point precision is used for entire implementation. As Wi-MAX is used for Metropolitan Area Network, it uses Orthogonal Frequency Division Multiple Access scheme.

References

- Erling H. Wold "Pipelined and Parallel-pipelined FFT FFT processor for VLSI Implementation" 0018-9340/84/0500-0414$01.00 © 1984 IEEE
- Hyun-Yong Lee, In-Cheol Park "Balanced Binary-Tree Decomposition for Area-Efficient Pipelined FFT Processing" 8328/$25.00 © 2007 IEEE
- Chin-Long Wey, Wei-Chien ang and Shin-Yo Lin "Efficient VLSI Implementation of Memory-Based FFT processors for DVB-T Applications" IEEE Computer Society Annual Symposium on VLSI(ISVLSI'07)
- Simeng li, Huxiong Xu, Wenhua Fan, Yun Chen, Xiaoyang Zeng 2010 "A 128/256-Point Pipeline FFT/IFFT Processor for MIMO OFDM System IEEE 802.16e" 978-1-4244-5309-2/10/$26.00 ©2010 IEEE

**Index Terms**

Computer Science  
Signal Processing

**Keywords**  
FFT  IFFT  Pipelined Architecture  SDF  Wi- MAX