Abstract

This paper describes the design and circuit simulation of split level charge recovery logic (SCRL). In conventional circuits the bits are thrown away for every transformation in the output level, and their associated energy becomes heat, which directly affects the cost of computation by increasing the system overhead required to get rid of the heat causing inconvenience of weight, short battery life etc. SCRL adiabatic logic promises to be an efficient technique to design low power digital VLSI circuit. The power efficiency of SCRL circuit is observed by comparing its performance with static CMOS inverter. A power efficient SCRL CLA is also designed and verified in this paper. Computer simulation using LTSPICE4 is carried out on SCRL circuit's implemented using CMOS technology.

References

Adiabatic Split Level Charge Recovery Logic Circuit


Index Terms

Computer Science

Circuits And Systems

Keywords

Low power  adiabatic Logic