Abstract

A low power analysis of the jitter bounded is presented in this paper. Digital Delay Locked Loop (DLL) are commonly used for clock synchronization in modern ICs because of their superior stability and process portability. The DLL has a graduated course delay line and a phase interpolating fine delay line.

References


Survey on Various Types of Power in DLL

2, Feb 2009, pp. 254–262.

Index Terms

Computer Science Circuits And Systems

Keywords

All digital delay locked loop (ADDLL) clock generator Jitter agilent E4422B
Oscilloscope 54833D