Abstract

High speed and low power multiplier circuits are highly demanded in VLSI design. In this paper, a new approach for high speed and low power multiplier design with less number of gate counts is proposed. In the Ripple Counter–based multiplier design, the number of computational clock cycles is reduced to n for n * n multiplication where n is the word length or the number of bits, which was 2n in the conventional CSAS multiplier. The Ripple Carry Adder (RCA) in the Counter-based design is replaced with Kogge-Stone adder (KSA) for reducing the average connection delay. For reducing the total equivalent gate count and power, the full adder with alternate logic is implemented along with KSA in the multiplier architecture. In our paper, 27.21% and 31.53% of the total power has been reduced for unsigned and signed number multiplication respectively.

References

Efficient Serial Multiplier Design using Ripple Counters, Kogge-Stone Adder and Full Adder

- S. Ghosh et al., "Tolerance to small delay defects by adaptive clock
Efficient Serial Multiplier Design using Ripple Counters, Kogge-Stone Adder and Full Adder


**Index Terms**

Computer Science

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**Keywords**

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