An Energy Efficient Set Associative Cache Algorithm

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Abstract

Set associative caches have fixed ways. Entire cache is enabled during cache operation. This paper proposes cache architecture mapping cache line to fixed cache way of mapped set. The address is mapped to set as in conventional set associative cache. The tag value of the mapped line is divided into blocks of size of number of cache ways. The average of maximum and minimum frequency of this division is the mapped way. The proposed model is simulated with SPEC2K benchmarks. The average memory access time degradation of 3.8% is seen over traditional set associative cache. The energy saving of 49% is observed in proposed model.

References

Index Terms

Computer Science
Algorithms

Keywords
Average memory access time  Energy savings  Set associative cache