Abstract

This paper presents 16×16 bit Radix-4 Modified Booth’s Multiplier (MBM) optimized for high speed multiplication by using pipeline Technique. This paper aims at reduction of hardware utilization. This is accomplished by the use of 3:2 compressor adders. An efficient VHDL code has been written, successfully simulated on Modelsim 10.2 simulator and Xilinx 12.4 navigator is used for synthesizing the code. Simulation result shows the clock period of 2.689ns. The selected device to synthesize the code is xc3s500e-4pq208 of Sartan-3E family. The area utilization is shown as 222 numbers of slices and 383 numbers of LUTs.

References

Implementation of Modified Booth Multiplier using Pipeline Technique on FPGA

- Chetan Gupta, "Design and implementation of a 32 bit MAC unit with pipelined variable stage Carry Select Adder"; Electronics Dept., Thapar University, June 2012.

Index Terms

Computer Science
Digital Circuits

Keywords
Compressor
Modified Booth Recoding
Pipelining
Radix-4
Xilinx navigator