Abstract

A new class of cyclic codes that is Reed-Solomon codes are discussed for IEEE 802.16 wireless networks. Reed-Solomon codes are used for the error detection and correction in communication systems. This is important in information theory and coding to correct burst errors. Here Reed-Solomon code for wireless network 802.16 is synthesized using VHDL on Xilinx and simulated on ISE simulator. The Reed-Solomon encoder has been checked for different error-correcting capabilities that is 4, 6, 8 etc. Reed-Solomon decoder for IEEE 802.16 network is synthesized on VHDL for error detection and correction. Here pipelining is introduced in Reed-Solomon decoder to improve the performance. The performance of Reed-Solomon encoder RS (255,239) for IEEE 802.16 is shown and Reed-Solomon decoder is checked for both RS(255,243) and RS(255,239) and synthesizable on FPGA.
FPGA Implementation of Reed-Solomon Encoder and Decoder for Wireless Network 802.16

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Index Terms

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