Abstract

Context-based adaptive variable-length coding (CAVLC) is an important feature of the latest video coding standard H. 264/AVC. The coding technique using conventional CAVLC based on area efficient design, the second is on low power design architecture will lead to low throughput. In this paper, an efficient CAVLC design is proposed. The main concept is the FPGA based pipelining scheme for parallel processing of two 4x4 blocks. When one block is processed by the scanning engine to collect the required symbols, its previous block is handled by the coding engine to translate symbols into bit stream. Our block based pipelined architecture doubles the throughput of CAVLC at high bit rates. The proposed architecture can make a real time processing of 1920X1080 @ 30fps. With the synthesis constraint of a 200MHz clock using altera cyclone-II FPGA.

References

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Index Terms

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