Abstract

Speech signals are often contaminated with acoustic noise, which is present in a variety of listening environments. This problem is of critical importance because background noise is particularly damaging to speech intelligibility for people with hearing loss and hearing aids users. A pre-processing step in modern digital hearing aids is denoising to estimate the signal in the band of interest from the available noisy signals without altering it. Advances in digital signal processing have allowed adding vital features to improve the performance of assistive listening devices like speech enhancement and noise reduction. Furthermore, the progress in field programmable gate arrays (FPGA) technology, especially for miniaturized system applications facilitated the implementation of small, portable and high performance devices. In this paper a signal processing core based on stationary wavelet packets is designed for speech enhancement and denoising in hearing aids. The developed core is implemented on FPGA and interconnected with embedded microprocessors and related peripherals to form a complete system on a programmable chip. The embedded software processor is Micro Blaze soft core processor. The chip used is Diligent XUP II Virtex-II Pro system FPGA containing audio codec LM4550. The features of the proposed design are intelligibility, small area and low cost.


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Index Terms

Computer Science

Applied Sciences

Keywords

denoising  hearing aids  FPGA  Micro Blaze  LM4550  stationary wavelet transform  wavelet packets