Abstract

To achieve high throughput in wireless networks a partial parallel LDPC decoder is proposed in this paper. For fully-parallel decoders, it suffers from large hardware complexity caused by a large set of processing units and complex interconnections. In wireless networks coding complexity and routing congestion can be reduced by designing the decoder with partially-parallel architecture. The partially-parallel architecture with Split Row algorithm reduces the total global wire length by about 26% without any hardware overhead and increasing the throughput by 60% and 71% in wireless networks.

Index Terms

Computer Science
Circuits And Systems
Keywords
LDPC-Low Density Parity Check Decoder  VN-Variable Node  PU-Processing Unit
WNs-Wireless Networks
CHNU-Check Node Unit
CNU-Control Node Unit
MU-Memory Unit
AGU-Automatic Gain Unit
SNR-Signal to Noise Ratio
SP-Split
Col-Column
Mem-Memory
BER-Bit Error Rate