Abstract

Digital sub-threshold circuits are significant for ultra-low power (ULP) applications. Operating circuits at ultra-low voltage levels leads to the less power per operation. An optimized method is separating the logic blocks based on performance requirement and utilizing multiple-supply voltage (VDD) for each blocks. In order to prevent an enormous static current in these multi-VDD circuits, voltage level converters are required. The advantages of single-supply level converter (SSLC) over dual-supply level converter (DSLC) are on the grounds of pin count, congestion in supply routing, complexity and overall system cost. In this paper, a novel sub-threshold single-supply voltage level converter (S_SSLC) based on dynamically-controlled body biasing technique is presented. In this work, a dynamically-controlled body biasing is utilized for setting the threshold voltages of the transistors in order to reduce the delay. This dynamic design can convert an input signal at sub-threshold/super–threshold region ranging from 0.3V-1.2V to 1.2V as output. Simulation results at 180nm CMOS technology node demonstrate the superiority of the proposed design compared to the conventional SSLC designs.
References


Index Terms

Computer Science

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Keywords

Digital sub-threshold circuits  ultra-low power  single-supply level converter  dynamically-controlled body biasing technique