This paper presents a fast multi-rate structure of Daubechies polyphase decimator which is required in the development of telecommunications systems and real time processing. It is an optimized approach which offers an increased efficiency in both size and speed, aspects that are well suited to reconfigurable architecture task heretofore implementation in FPGA platform which offers the potential of designing high performance systems at low cost. Hence, in order to evaluate the features of this method and to check the proposed extension of the basic Daubechies wavelet with four coefficients, a computer simulation was performed. It always simple and quick testing of the algorithm behavior of the proposed method for a wide class of signal processing. The Matlab/Simulink package and Modelsim were chosen as the programming environments for computer simulations.
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Index Terms

Computer Science

Digital Signal Processing

Key words

Daubechies wavelet

Filter Decimator

Multirate

system

Altera FPGA

Xilinx FPGA

Modelsim

Matlab/simulink