Abstract

Network on Chip is efficient on-chip communication architecture for system on chip architectures. It enables the integration of a large number of computational and storage blocks on a single chip. The router is the basic element of NoC. The router architecture can be used for building a NoC with standard topology with low latency and high speed. In this paper, we implement and analyze a 3x3 mesh network configuration with routers which can support simultaneous routing requests, with blocking and non blocking inputs.

References

Analysis of Mesh Topology of NoC for Blocking and Non-blocking Techniques

- Xilinx Inc. www.xilinx.com

Index Terms
Computer Science Communication Networks

Keywords
Network on Chip (NoC) Flit Finite State Machine (FSM) Router Architecture packet