Abstract

In most of the digital circuits, CMOS based design is allowed to be used in practice. Generally, CMOS stands for Complementary Metal Oxide Semiconductor Field Effect Transistor, that is, considered to be as combination of both PMOS as well as NMOS. In CMOS based design, symmetry should be followed in circuit operation. Most of the complex circuits are allowed to design in CMOS, however, there are several drawbacks present in this complementary based design. Also, SRAM cell read stability and write-ability are major concerns in nanometer CMOS technologies, due to the progressive increase in intra-die variability and supply voltage scaling. Therefore, it is necessary to find alternative way suitable for particular design, instead of CMOS. Most of the modern design is based on Carbon nanotube FET or FinFET because of its superior properties interms of power consumption, leakage power, delay etc. The objective of this work mainly focus on designing 6-T SRAM cell in 32nm CMOS, CNTFET as well as FinFET and finally, to compare the parameters such as average power, delay and leakage current.

References

- Michael Wieckowski, Sandeep Patil, and Martin Margala,” Portless SRAM—A


- Azeez Bhavnagarwala, Stephen Kosonocky, Carl Radens, Kevin Stawiasz, Randy Mann, Qiuyi Ye, Ken Chin, ” Fluctuation Limits & Scaling Opportunities for CMOS SRAM Cells”, IEEE, 2005.


- Eric Chin, Mohan Dunga, Borivoje Nikolic,” Design Trade-offs of a 6T FinFET SRAM Cell in the Presence of Variations”,


Index Terms

Computer Science Circuits And Systems

Keywords

Carbon nanotube CMOS Data Retention FinFET Static RAM