Abstract

In this paper we discuss Hybrid Ripple Carry Lookahead Adder (HRCLA), which is a hybrid between Carry Lookahead Adder (CLA) and ripple adder (RA). In HRCLA time is traded off for area and power. HRCLA has been designed by rippling the last carry bit of a 4-bit CLA. HRCLA extracts the traits of Carry Lookahead Adders (CLA) speed and ripple adders (RA), area. A four bit proposed HRCLA has been implemented in Cadence using 45nm technology; the implementation results showed 12.2 %Area, 4.6 % power improvement and 14.01 % critical path delay overhead over CLA.
Reduced Complexity Hybrid Ripple Carry Lookahead Adder

Bureau of Standards, Circ. 591, 1958, pp: 3-12.

Index Terms

Computer Science

Circuits And Systems

Keywords

Ripple Adder  Carry Lookahead Adder (CLA)  Hybrid Ripple Carry Lookahead Adder (HRCLA)