Abstract

Two modified architectures for modulo 2n+1 adders are introduced in this paper. Only some of the carries of modulo 2n+1 addition are computed in sparse carry computation unit present in first architecture. This sparse approach is introduced by inverted circular idempotency property of the parallel-prefix carry operator and in this modified pre-processing stage and carry select blocks are combine the multiplexer operation of a diminished-one adder can be implemented in smaller LUTs and less consumes power, while maintain the same operating speed and delay. The modulo adder 2n+1 adders can be easily derived by adding extra logic of modulo 2n-1 adders present in second architecture.

References

- www.cs.kent.edu/~rothstei/modular_arith.ppt
Analysis of Power Efficient Modulo 2n+1 Adder Architectures


Index Terms

Computer Science

Circuits And Systems

Keywords

Parallel-Prefix-Addition  IEAC  Modulo- Arithmetic  Boolean Expression  VLSI