Abstract

This paper describes the prototyping of a BCH (Bose, Chaudhuri, and Hocquenghem) code using a Field Programmable Gate Array (FPGA) reconfigurable chip. BCH code is one of the most important cyclic block codes. Designing on FPGA leads to a high calculation rate using parallelization (implementation is very fast), and it is easy to modify. BCH encoder and decoder have been designed and simulated using MATLAB, Xilinx-ISE 10. 1 Web PACK and implemented in a xc3s700a-4fg484 FPGA. In this implementation we used 15 bit-size code word and 5 bits data, any 3 bits error in any position of 15 bits has been corrected. The results show that the system works quite well.

References

- A. S. Das, S. Das, and J. Bhaumik &quot;Design of RS (255,251) Encoder and Decoder in FPGA&quot;; international journal of soft computing and engineering, Volume- 2,
FPGA Implementation of 3 bits BCH Error Correcting Codes

Issue-6, January 2013.

**Index Terms**

- Computer Science
- Communications

**Keywords**

- Error correcting codes
- BCH codes
- encoding
- decoding
- FPGA