Abstract

This paper presents an effective approach to estimate tree interconnect delays in VLSI circuit designs in deep submicron technologies at high frequencies. In this paper, a symmetrical multi-level interconnect tree network topology has been taken up which consists of elementary resistance, inductance in series with capacitance in parallel. A precise method of modeling symmetrical T-tree interconnect network is effectively examined in this paper. By moment matching fine results are obtained at frequencies as high as 2 GHz at 180 nm technology node.
Delay Minimization in Multi Level Balanced Interconnect Tree


**Index Terms**

Computer Science

Algorithms

**Keywords**

Balanced tree delay moment matching multi-level interconnect VLSI