Abstract

This paper presents an effective approach to estimate tree interconnect delays in VLSI circuit designs in deep submicron technologies at high frequencies. In this paper, a symmetrical multi-level interconnect tree network topology has been taken up which consists of elementary resistance, inductance in series with capacitance in parallel. A precise method of modeling symmetrical T-tree interconnect network is effectively examined in this paper. By moment matching fine results are obtained at frequencies as high as 2 GHz at 180 nm technology node.

References

Delay Minimization in Multi Level Balanced Interconnect Tree

- Ismail, Y. I. ; Friedman, E. G. , &quot;Effects of inductance on the propagation delay and repeater insertion in VLSI circuits,&quot; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol. 8, no. 2, pp. 195,206, April 2000.
- Xiao-Chun Li; Jun-Fa Mao; Hui-Fen Huang, &quot;Accurate analysis of interconnect trees with distributed RLC model and moment matching,&quot; Microwave Theory and Techniques, IEEE Transactions on , vol. 52, no. 9, pp. 2199,2206, Sept. 2004.

Index Terms

Computer Science

Algorithms

Keywords

Balanced tree delay moment matching multi-level interconnect VLSI