Abstract

Rapid advances in the field of very large scale system designs brought memory circuits are continuously regulated and in turn, more number of cells could made possible to integrate on small chip. CMOS technology prove boon to memory circuits, which replaced the most of complex circuits to simpler circuits. But the combination of bipolar junction transistors changes the entire scenario. The objective of this paper is to design low power SRAM cell array by using BiCMOS technology. In this paper, BiCMOS technology is used to design SRAM cell using 0.18µm technology. The results are compared with standard 6T SRAM cell. The proposed design results in significant reduction in power consumption as compared to standard 6T SRAM cell and it is verified that the proposed cell can operate at much low supply power with much reduction in power consumption. All the simulation is completed on the Cadence Virtuoso tool.

References

- Takada, M. Nakamura, K.; Yamazaki, T. 1995 High speed submicron BiCMOS
- Hirdaya Narain Mishra and Yashwanta Kumar Patel. 2010 Design, Simulation and Characterization of Memory Cell Array for Low Power SRAM using 90nm CMOS Technology. IEEE.
- Masataka Matsui, Hiroshi Momose, Yukihiro Urakawa, and et. al. 1989 An 8ns 1Mb ECL BiCMOS SRAM&qu Address of the corresponding author.
- Sheriff ATawfik and Volkan Kursun. 2008 Low power and robust 7T dual Vt SRAM circuit. IEEE, 1452 to 145.

Index Terms

Computer Science
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Keywords

BiCMOS SRAM  Standard 6T SRAM  Power Consumption  Power Dissipation and 0.18µm technology