Abstract

This paper deals with the design opportunities of Static Random Access Memory (SRAM) for lower power Consumption and propagation delay. Here we have analyzed both read margin for read ability and write margin for SRAM write ability. Static Noise Margin affects both read margin and write margin. We have analyzed the Static Noise Margin using traditional butterfly method which requires the rotation of VTC by 45 degrees. SRAM cell is analyzed through the considering of different type of analysis such as Static Noise Margin, Data Retention Voltage, Read Margin and Write Margin in 350nm technology.
SRAM Cell Performance in Deep Submicron Technology

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**Index Terms**

Computer Science

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**Keywords**

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