Abstract

In present scenario high speed and low power devices in signal processing system is generally needed the efficient design and reduced complexity of converters, therefore conventional flash ADC is not fully meet the required specifications. ADC with high speed and low resolution is required in present communication technologies. Lower leakage current with low power consumption is considerable effect for different parameter optimization of flash ADC. The approach for reducing the leakage current is stacking power gating technique in three modes sleep, active and sleep-to-active modes. The design circuit has been simulated using cadence virtuoso tool with 45nm CMOS technology at various supply voltages. Ground bounce noise reduction has been done in flash ADC with stacking power gating approach to reduce the leakage current and active power.

References

Analyzing the Impact of Stacking Power Gating Technique on Ground Bounce Noise Effect of 3-Bit Flash Analog to Digital Converter

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Analyzing the Impact of Stacking Power Gating Technique on Ground Bounce Noise Effect of 3-Bit Flash Analog to Digital Converter


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