Abstract

In the design of Integrated circuits, area plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in many data-processing processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is reducing the area of CSLA based on the efficient gate-level modification. In this paper 4 bit, 8 bit, 16 bit, 32 bit, 64 bit and 128 bit Regular Linear CSLA, Modified Linear CSLA, Regular Square-root (SQRT) CSLA and Modified SQRT CSLA architectures have been developed and compared the area of these 4 types of CSLA and also applied these 4 bit, 8 bit, 16 bit, 32 bit, 64 bit and 128 bit CSLAs into 4X4 bit, 8X8 bit, 16X16 bit, 32X32 bit, 64X64 bit and 128X128 bit Vedic Multiplier (VM) respectively, then compared the area of Vedic Multiplier based on this adders. However, the Regular CSLA is still area consuming due to the dual Ripple Carry Adder (RCA) structure. For reducing the area of CSLA, it can be implemented by using a single RCA and an add-one circuit instead of using dual RCA. Comparing the Regular CSLA with Modified CSLA, the Modified CSLA has less area. The results and analysis show that the Modified SQRT CSLA provides better outcomes like less area and also the Vedic Multiplier using Modified Linear CSLA provides less area. This project was aimed for implementing high performance optimized FPGA architecture. Modelsim 10. 0c is used for simulating the CSLAs and VM using CSLAs and synthesized using Xilinx PlanAhead13. 4. Then the implementation
Implementation and Comparison of Vedic Multiplier using Area Efficient CSLA Architectures is done in Virtex FPGA Kit.

References


Index Terms

Computer Science Integrated Circuits
Keywords

Area efficient  Binary to Excess-1 Converter (BEC)  Carry Select Adder (CSLA)
Field programmable Gate Array (FPGA)

Linear CSLA

Square-root CSLA (SQRT CSLA)

Vedic Multiplier (VM)

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