Abstract

Reversible logic is becoming one of the best emerging design approaches for future computation of reversible logic having its more application in low power application. This logic is applied in the quantum computers, optical computing, communication and nanotechnology. In reversible logic approach generates the garbage input/output. In this paper design of proposed reversible logic multiplexer with garbage input/output, that the low power, area design technique are using that is the Gate -Diffusion -Input (GDI cell) in this dynamic component of power is reduced, In GDI cell PMOS is not connected to supply voltage VDD and NMOS is not connected to the GND. GDI circuits provide some measure issues of enhanced hazard tolerance and low voltage operation of reversible logic circuits. In this paper propose a novel application of GDI (Gate-Diffusion Input) circuits to Reversible logic multiplexer with its Garbage input and output. The new proposed design technique will consume less power than the other traditional gate. In recent years ago reversible logic circuit is less power dissipation. This GDI cell technique reduces the power of the circuit, delay, Power-Delay Product (PDP) and it also reduced frequency. The device scaling is limited by the power dissipation are more optimize in terms of delay, power supply, frequency , duty cycle, frequency jitter bandwidth of the signal
and also demonstrated the noise of the circuit. The proposed reversible logic design is effective in low power, low leakage current and lower Delay. The transistor implementation of the proposed gates is done by using Virtuoso tool of cadence. Based on simulation results and analysis at 45 nm technology, some of the trade-offs are made in the design to improve the efficiency.

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Index Terms

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Keywords

Low Leakage power  GDI technique  delay  (Power-Delay Product) PDP and frequency