Abstract

The paper describes the additional proven techniques for creating highly effective testbenches. This paper presents topics that are likely to be used by most test-benches. Samples of the techniques, as well as the underlying concepts, are presented. The paper shows several ways to use VIP with OVM technology and provides the knowledge to customize, modify, and extend the techniques to suit the needs of SoC designers. The basic steps to create a first constrained random testbench with VIP and OVM is also presented. It can be a template to develop more complex and powerful test-benches using other computing methods and features of OVM and VIP.

References

- Bryan Ramirez, Michael Horn; Parameters and OVM - Can't They Just Get Along? Proceedings of Design and Verification Conference & Exhibition (DVCon 2011).
- Stephen D'Onofrio, Ning Guo; Building reusable verification environments with OVM; proceedings of EDA Tech Design Forum - 08, pp. 1-9, 2008.
- Mikhail Chupilko, A. Kamkin; A TLM-Based Approach to Functional Verification of Hardware Components at Different Abstraction Levels; Proceedings of the IEEE Conference, Test Workshop (LATW), pp. 1-6, 2011.
- Rudra Mukherjee, Sachin Kakkar; Towards an Object-Oriented Design Methodology using SystemVerilog; Proceedings of Design and Verification Conference & Exhibition (DVCon 2009), pp. 234-239, 2009
- System Verilog Testbench Constructs; www.testbench.in

**Index Terms**

Computer Science  
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**Keywords**

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