Abstract

The paper describes the additional proven techniques for creating highly effective testbenches. This paper presents topics that are likely to be used by most test-benches. Samples of the techniques, as well as the underlying concepts, are presented. The paper shows several ways to use VIP with OVM technology and provides the knowledge to customize, modify, and extend the techniques to suit the needs of SoC designers. The basic steps to create a first constrained random testbench with VIP and OVM is also presented. It can be a template to develop more complex and powerful test-benches using other computing methods and features of OVM and VIP.

References

Advanced Testbench Design using Reusable Verification Component and OVM

- Bryan Ramirez, Michael Horn "Parameters and OVM - Can't They Just Get Along?". Proceedings of Design and Verification Conference & Exhibition (DVCon), 2011.
- "System Verilog Testbench Constructs". www.testbench.in

Index Terms

Computer Science
Software Engineering

Keywords
Open Verification Methodology Verification Intellectual Property System on Chip Design Under Test
Transaction Level Modeling