Abstract

Digital Signal Processing (DSP) algorithms always have a need for calculating certain linear, trigonometric, hyperbolic, logarithmic and other transcendental functions. CORDIC based algorithms have long been used in evaluating these functions. Traditional approaches have, however, been limited to software domain only. The simplicity of operation of CORDIC algorithm encourages its implementation in hardware. In this paper a novel CORDIC architecture for sine and cosine function evaluation has been proposed. The hardware integration is carried out using Field Programmable Gate Arrays (FPGAs). The proposed algorithm is based on modified carry save addition and incorporates bit-truncation. The structure offers extremely low latency and high operating frequencies, when pipelined. The novelty of the proposed architecture is that it offers a flat timing response for varying input word lengths. The structure has an inherent capability of supporting an additional internal pipeline within each stage, enabling the structure to operate at high frequencies, typically four times that of the normal CORDIC. The performance analysis is carried out by comparing the proposed architecture against existing non-redundant (basic) and redundant (modified) architectures.
References


Index Terms

Computer Science
Signal Processing

Keywords

Carry save Addition
CORDIC Algorithm
Digital Signal Processing
FPGA
Pipelining
Rotation Mode