Abstract

In this paper, new hardware architecture of multiplier and accumulator (MAC) for high speed arithmetic was designed. The performance was improved by merging multiplication with accumulation and organize a hybrid type carry save adder (CSA). The proposed CSA tree uses 1's complement based radix-4 and radix-8 modified booth algorithm (MBA). The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to reduce the number of the input bits of the final adder. This MAC add the intermediate results in the form of sum and carry bits instead of the final adder output, which made it possible to optimize the pipeline system to improve the performance. The final addition was carried out by high speed carry select adder (CSLA) with binary to excess converter using CLA. Based on the theoretical and experimental estimation, we analyzed the results in terms of delay. The design is implemented using VHDL language and simulated using Xilinx ISE10.1 Simulator.

References


- G. A. Ruiz1 and Mercedes Granda, "Efficient hardware implementation of 3X for radix-8 encoding"; Proc. of SPIE Vol. 6590 65901I-1

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