Abstract

In high speed ADC, comparator influences the overall performance of ADC directly. This paper describes a very high speed and high resolution preamplifier comparator. The comparator uses a self-biased differential amp to increase the output current sinking and sourcing capability. The threshold and width of the new comparator can be reduced to the millivolt (mV) range, the resolution and the dynamic characteristics are good. Based on UMC 0.18um CMOS process model, simulated results show the comparator can work under a 25dB gain, 55MHz speed and 210.10µW power.

References

High Speed and High Resolution Self Biased Differential Amplifier based Latch Comparator


- N. Stefanou and S. R. Sonkusale, "An average low offset comparator for 1.25G samples/s ADC in 0.18 um CMOS", IEEE ECAS.


**Index Terms**

Computer Science

Networks

**Keywords**

High speed ADC high speed comparator high resolution and preamplifier latch comparator